

**INTEGRATED CIRCUIT WITH MODIFIED
METAL FEATURES AND METHOD OF FABRICATION THEREFOR**

Abstract

5 Embodiments of the invention concern modifying the layout of one or more
metal layers of an integrated circuit before patterning those layers, so that an intermetal
dielectric layer (IDL) subsequently deposited over the top surface of the patterned layer
will be substantially self-planarized. The spacing between parallel edges of adjacent
first metal lines and features is standardized, and one or more additional metal features
10 are included in areas where an intersection exists. The additional metal features serve to
maintain the elevation of the top surface of the IDL at the same height across the
intersections, thus achieving self-planarization across the entire top surface of the IDL,
without the need for a thicker than desired IDL. The modified metal layers are adapted
for use in conjunction with memory cells and apparatus incorporating such memory
15 cells, as well as other integrated circuits.

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